Recent Progress in High-k Dielectric Investigation for DRAM Capacitor Application Deposited by Atomic Layer Deposition

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Capacitor in dynamic random access memory (DRAM) device, one of the key component which dominantly governs the characteristics of the device, requires a deposition process for obtaining conformal film thickness in a structure with extremely high aspect ratio from decreased design rule. In this regard, atomic layer deposition (ALD) technique has been employed as a solely solution for DRAM capacitor dielectric deposition due to its self-limiting nature. Moreover, a trade-off relationship between capacitance density and leakage current density as a consequence of the inherent characteristics of high-k dielectric, a material higher dielectric constant generally has smaller bandgap, derives a lot of attentions about the investigation on ALD process for high-k dielectric materials to overcome or compensate this limitation for demonstrating improvement of DRAM capacitor.

In this talk, the results about various approaches to enhance the properties of dielectric thinfilm deposited by ALD for the capacitor application will be introduced. The investigations about the leakage current conduction mechanism depending on employed dielectric material, electrode and several following processes, will be discussed. Several suggested method to improve the capacitance density will be discussed, as well.